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- Members of the Texas Instruments
 Widebus™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Bus-Driving True Outputs
- Flow-Through Architecture Optimizes
 PCB Layout
- Distributed Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC[™] (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

description

The SN54ACT16374 and 74ACT16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54ACT16374 . . . WD PACKAGE 74ACT16374 . . . DL PACKAGE (TOP VIEW)

10E	1	48]1CLK
1Q1 [2	47] 1D1
1Q2 [3	46] 1D2
GND [4	45	GND
1Q3 [5	44] 1D3
1Q4 [6	43] 1D4
v _{cc} [7	42]v _{cc}
1Q5 [8	41] 1D5
1Q6 [9	40] 1D6
GND [10	39] GND
1Q7 [11	38] 1D7
1Q8 [12	37] 1D8
2Q1 [13	36	2D1
2Q2 [14	35] 2D2
GND [15	34]GND
2Q3 [16	33] 2D3
2Q4 [17	32]2D4
Vcc[18	31]v _{cc}
2Q5 [19	30] 2D5
2Q6 [20	29]2D6
GND [21	28] GND
2Q7 [22	27] 2D7
2Q8	23	26]2D8
20E	24	25]2CLK
			l

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

An output-enable input (\overline{OE}) can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state provides the capability to drive bus lines in a bus-organized system without need for interface or pullup components. \overline{OE} does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16374 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit board area.

The SN54ACT16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16374 is characterized for operation from –40°C to 85°C.



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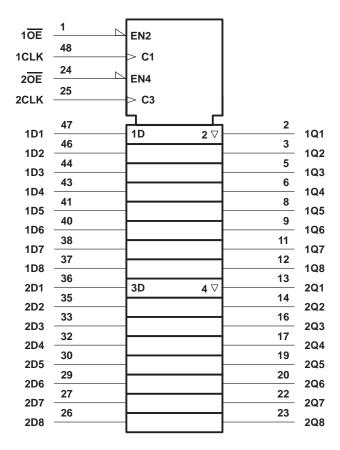


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FUNCTION TABLE (each section)

	INPUTS	OUTPUT	
ΘE	CLK	D	Q
L	1	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q ₀
Н	Χ	Χ	Z

logic symbol†

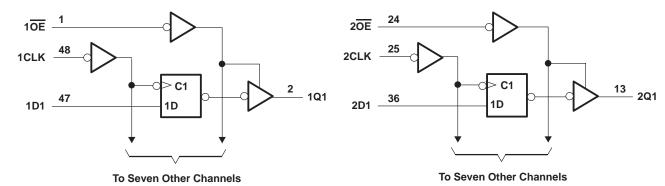


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±400 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2): DL package	1.2 W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 3)

		SN54ACT16374			74	ACT1637	74	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage (see Note 4)	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
٧ _I	Input voltage	0		VCC	0		VCC	V
Vo	Output voltage	0		VCC	0		VCC	V
loh	High-level output current			-24			-24	mA
loL	Low-level output current			24			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	0		10	ns/V
TA	Operating free-air temperature	-55		125	-40		85	°C

NOTES: 3. Unused inputs must be held high or low to prevent them from floating.

4. All V_{CC} and GND pins must be connected to the proper voltage supply.



^{2.} The maximum package power dissipation is calculated using a junction temperature of 150 °C and a board trace length of 750 mils.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	T,	Δ = 25°C	;	SN54AC	Γ16374	74ACT	16374	UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		
	ΙΟΗ = -30 μΑ	5.5 V	5.4			5.4		5.4		
.,	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		.,
VOH	10H = -24 IIIA	5.5 V	4.94			4.7		4.8		V
	I _{OH} = -50 mA [†]	5.5 V				3.85				
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V						3.85		
	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
	ΙΟΣ = 50 μΑ	5.5 V			0.1		0.1		0.1	٧
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
VOL	10L - 24 111A	5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V					1.65			
	$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V							1.65	
lį	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
ΔlCC [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1		1	mA
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
Co	V _O = V _{CC} or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T _A =	T _A = 25°C		SN54ACT16374		16374	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	ock frequency				65	0	65	MHz
	Pulse duration	CLK low	7.5		7.5		7.5		
t _W	ruise duration	CLK high	4.5		4.5		4.5		ns
t _{su}	Setup time, data before CLK↑	6.5		6.5		6.5		ns	
th	Hold time, data after CLK↑		1		1		1		ns

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

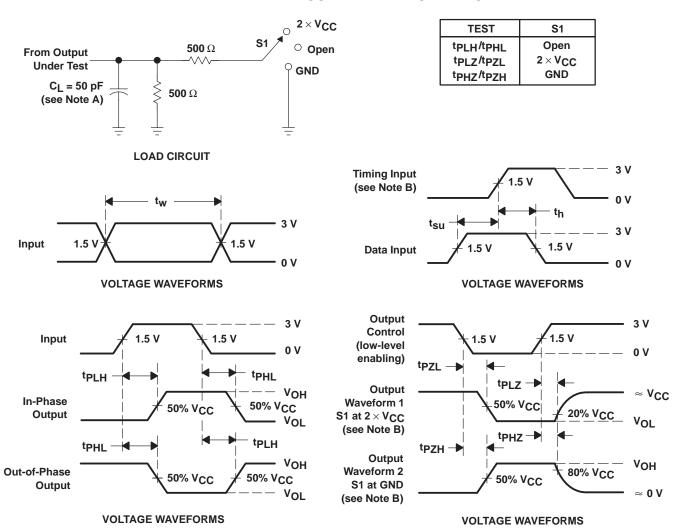
PARAMETER	FROM	то	T,	T _A = 25°C			SN54ACT16374		74ACT16374		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
f _{max}			65			65		65		MHz	
t _{PLH}	CLK	Q	5.1	8.8	10.9	5.1	13.2	5.1	12.4	ns	
tPHL	CLK	Q	5.3	8.8	10.9	5.3	13.1	5.3	12.2	115	
^t PZH		0	3.7	8.4	10.5	3.7	12.7	3.7	11.9	no	
tpzL	ŌĒ	Q	4.4	9.7	11.9	4.4	14.3	4.4	13.4	ns	
^t PHZ	ŌĒ	0	5.4	7.9	9.8	5.4	10.9	5.4	10.4	20	
tPLZ	OE	Q	4.9	7.2	9.1	4.9	10.2	4.9	9.8	ns	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	TYP	UNIT		
C _{pd}	Dower discinction conscitones per flip flep	Outputs enabled	C _I = 50 pF,	f = 1 MHz	52	pF
	Power dissipation capacitance per flip-flop	Outputs disabled	CL = 50 pr,	I = I IVINZ	38	

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 3 \ ns$, $t_f = 3 \ ns$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9202501MXA	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type
74ACT16374DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16374DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16374DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16374DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ACT16374WD	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	_	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1





*All dimensions are nominal

Ī	Device	Package Type	Package Drawing	age Drawing Pins		Length (mm)	Width (mm)	Height (mm)	
	74ACT16374DLR	SSOP	DL	48	1000	346.0	346.0	49.0	

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA

GDFP1-F56 and JEDEC MO-146AB

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